

CPRI v4.1 IP Cores

Product Brief

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Overview

CPRI (Common Public Radio Interface) is an interfacing standard for high-speed communication of digital radio and control data channels between wireless infrastructure base station inter-modules.

Radiocomp's CPRI v4.1 IP Cores solution enable the quickest and most flexible deployment of both REC (Radio Equipment Controller) and RE (Radio Equipment) interfaces. They include all features required to support WiMAX 802.16e-2005 and WCDMA/LTE applications. Radiocomp's CPRI Cores are complete and fully tested solution compliant with the latest CPRI v4.1 specifications and they are widely used today in many field installations.

Description

The CPRI IP Cores are compliant with the latest CPRI v4.1 specifications and support WCDMA/LTE and WiMAX Wireless standards in either REC or RE configuration. They constitute a complete solution for any FPGA or ASIC technology.

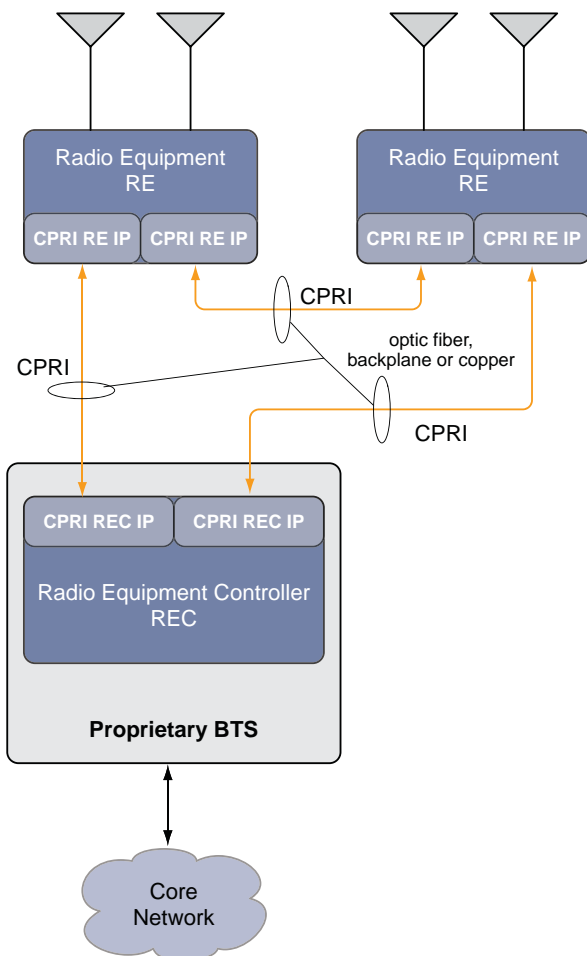
The cores can use either FPGA embedded or external transceiver devices to implement the Physical Layer (L1). The framer/de-framer (L2) and the upper layers (L3 and above) including IQ sample mapper/de-mapper, C&M interfaces, Ethernet and HDLC MAC, are implemented into the FPGA logic.

The C&M block supports access to both Fast (Ethernet) and Slow (HDLC) streams as well as direct handling of alarms via the CPU interface or via dedicated user logic. Synchronization signal I/Os are provided to enable synchronization of the communication with the BTS global timing.

The IP cores include an optimized fully integrated HDLC and Ethernet MAC 10/100 blocks that are fully configurable via the register interface (Avalon). Optionally, an external Ethernet MAC is supported via a GMII interface.

Accurate measurement and calibration of the link delay budget for synchronization recovery is fully supported.

The IP also supports various loop-back options such as Serial, Full Parallel, C&M and IQ. This enables effective link verification and debugging. The block-based and open interface structure makes it straightforward to integrate into existing designs.



Benefits

- Compact & complete package
- Ethernet and HDLC MAC layer included
- Support for multiple communications standards and any mapping method as defined in CPRI v4.1 specification
- Support for multiple CPRI line rates up to 6.144 Gbps with scrambling layer
- Simplified and quick implementation of CPRI interfaces for OEMs



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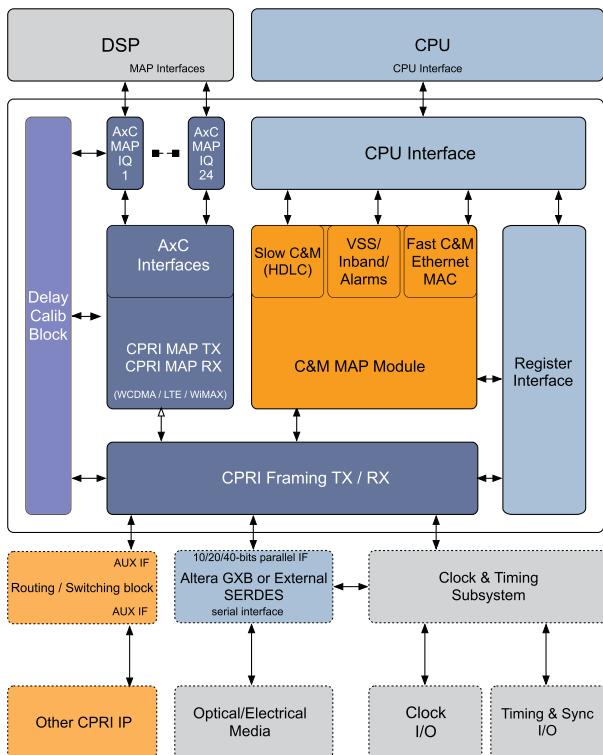
Technical Data Sheet

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IP Technical description

CPRI REC/RE Key Features

- 614.4 Mbps / 1.288 / 2.457.6 / 3.072 Gbps / 6.144 Gbps
- WiMAX and WCDMA/LTE mapping support. Mapping support for other standards is optional.
- Up to 24 IQ Interfaces
- Size optimized HDLC and Ethernet MAC 10/100 integrated. Optional direct GMII external interface is also available.
- Accurate Delay Measurement and Calibration Integrated



Interface Overview

- High Speed Serial Interface
Altera GXB, Xilinx MGT or external SERDES
- AxC MAP IQ Interfaces
Up to 24 antenna carrier interfaces according to the wireless standard used
- Auxiliary interface with low latency for daisy chaining
- Generic CPU interface enables register configuration and access to Ethernet 10/100 and HDLC channels. Optionally a GMII Ethernet interface can be used from external MAC
- HDLC Interface
Serial interface carrying HDLC frames to CPU or to dedicated logic
- Synchronization Interface I/Os
I/O used to process the BTS Global Timing in REC or recovered timing in RE
- Clock Interface I/Os

Delivery Package

- VHDL Encrypted source code or Netlist
- VHDL Test-bench with regression testing
- Hardware Interface Specification
- CPRI Test Specification
- User Manual

References

- CPRI v4.1 Specifications
- Radiocomp's CPRI Test Specification

Resource Usage Table

| | |
|------------------|------|
| Comb. ALUTs: | 6779 |
| Logic Registers: | 4288 |
| M512s: | 2 |
| M4K: | 22 |