

CPRI v4.0 IP Cores

Product Brief

Rev. 3.2 | Company Proprietary | 25th of may 2009



Overview

CPRI (Common Public Radio Interface) is an interfacing standard for high-speed communication of digital radio and control data channels between wireless infrastructure base station inter-modules.

Radiocomp's CPRI v.4.0 IP Cores solution enable the quickest and most flexible deployment of both REC (Radio Equipment Controller) and RE (Radio Equipment) interfaces. They include all features required to support WiMAX 802.16e-2005 and WCDMA/LTE applications. Other standards mapping support is available on demand. Radiocomp's CPRI Cores are fully tested and compliant with the latest CPRI v.4.0 specifications and they are widely used today in many field installations.

Description

The CPRI IP Cores are compliant with the latest CPRI v.4.0 specifications and support WCDMA/LTE and WiMAX Wireless standards in either REC or RE configuration. They constitute a complete solution for any FPGA or ASIC technology, and they are optimized to fit seamlessly into Altera Stratix IV GX, Stratix II GX, Arria GX and Cyclone III Altera FPGA devices.

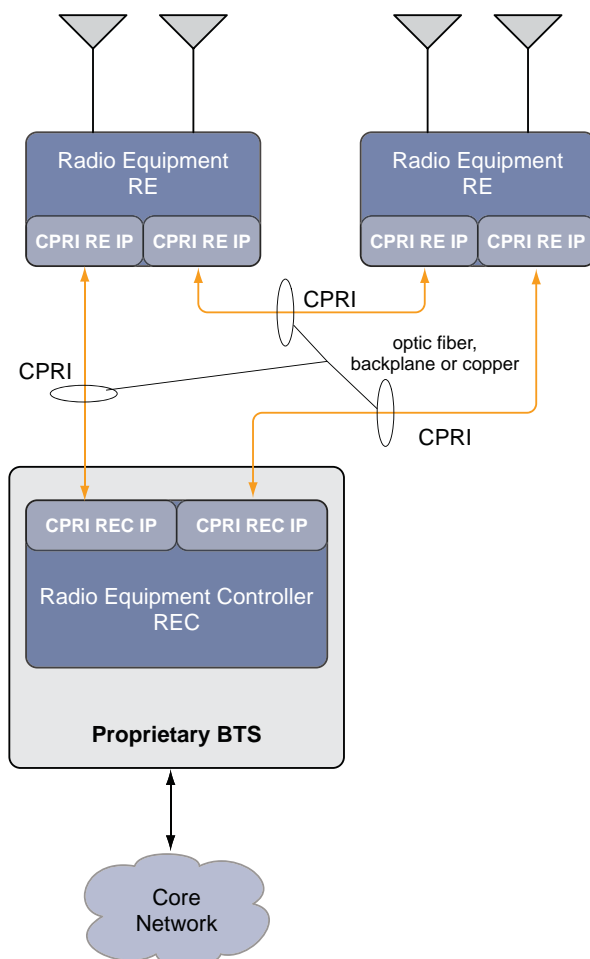
The cores can use either Altera GXB or external transceiver solutions to implement the Physical Layer (L1). The framer/de-framer (L2) and the upper layers (L3 and above) including mapper/de-mapper, C&M interfaces, and Ethernet MAC, are implemented into the FPGA logic. The IP Cores include mapper/de-mapper blocks for each wireless standard.

The C&M block supports both Fast (Ethernet) and Slow (HDLC) streams as well as direct handling of alarms via the CPU interface or via dedicated user logic. Synchronization signal I/Os are provided to enable synchronization of the communication with the BTS global timing.

The IP cores include an optimized and fully integrated Ethernet MAC 10/100 block that is fully configurable via the register interface (Avalon). Optionally, an external Ethernet MAC is supported via an MII interface.

Accurate measurement and calibration of the link delay budget for synchronization recovery is fully supported.

The IP also supports various loop-back options such as Serial, Full Parallel, C&M and IQ. This enables effective link verification and debugging. The block-based and open interface structure makes it straightforward to integrate into existing designs.



Benefits

- Compact & complete package
- Ethernet MAC layer included
- Support for multiple communications standards
- Support for multiple CPRI line rates
- Simplified and quick implementation of CPRI interfaces for OEMs

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Technical Data Sheet

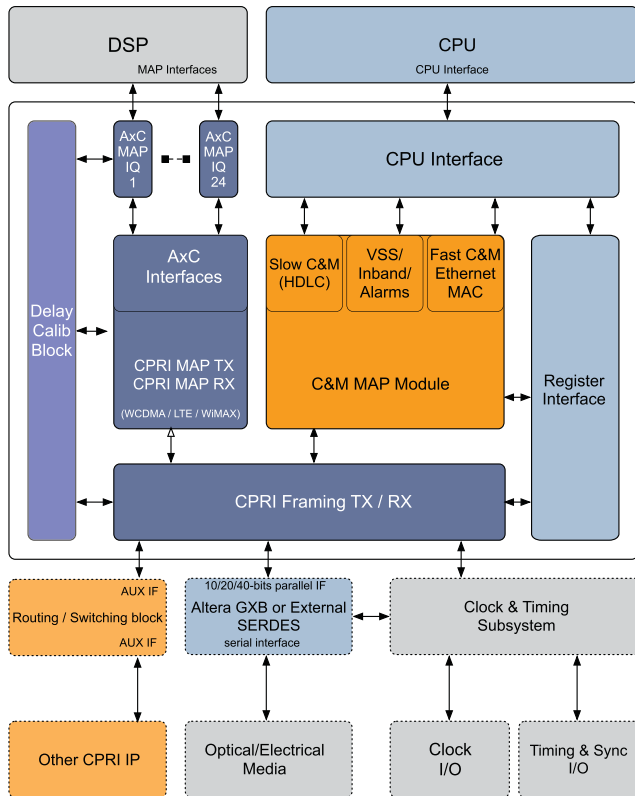
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IP Technical description

CPRI REC/RE Key Features:

- 614.4 Mbps / 1.288 / 2.457.6 / 3.072 Gbps / 6.144 Gbps (pre-standard)
- WiMAX and WCDMA/LTE mapping support. Mapping support for other standards is optional.
- Up to 24 IQ Interfaces
- Size optimized Ethernet MAC 10/100 integrated with optional direct MII external interface.
- Accurate Delay Measurement and Calibration Integrated



Resource Usage Table

Comb. ALUTs:	6.779
Dedicated logic registers:	4.288
M512s:	2
M4K:	22

Values are provided for the smallest number of antenna carrier interfaces defined by generic parameter NMAP = 1 (1 antenna carrier interface).

Interface Overview:

- High Speed Serial Interface
Altera GXB or external SERDES
- AxC MAP IQ Interfaces
Up to 24 antenna carrier interfaces according to the wireless standard used
- Access via CPU interface supporting 10/100 ethernet rates
Direct Avalon interface to CPU supporting 10/100 rates. Optionally an MII interface to external MAC is provided
- HDLC Interface
Serial interface carrying HDLC frame at 61.44 Mbps to CPU or to dedicated logic
- Channel access via CPU interface
Direct Avalon interface to CPU or dedicated logic
- Synchronization Interface I/Os
I/O used to process the BTS Global Timing in REC or recovered timing in RE
- Clock Interface I/Os

Delivery Package

- VHDL Encrypted source code or Netlist
- VHDL Test-bench
- Hardware Interface Specification
- User Manual

References

- CPRI v.4.0 Specifications

Resources Utilization

- The sizes below are according to a 16 antenna carrier interface configuration on Stratix II GX devices
- The size may vary according to other specific interface configurations

Optimized for



The CPRI 4.0 IP is optimized for Altera CycloneII, CycloneIII, Stratix IV GX and Arria GX, which devices names and logo all are registered trademarks of Altera Corporation.